TECHNICAL SPECIFICATION

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Logic digital integrated circuits – Specification for I/O interface model for integrated circuit (IMIC version 1.3)

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 62404, which is a technical specification, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
47A/746/DTS	47A/751/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

With an increase in speed of electronic systems, it becomes necessary to accurately predict electrical performance including noise in electronic systems with integrated circuits.

Simulators have been used for this purpose. Simulators need accurate models for describing electrical properties of integrated circuits. Semiconductor manufacturers and/or suppliers are required by their users to prepare device models for various simulation tools, some of which are not compatible with SPICE. In addition, since SPICE models contain proprietary process parameters, a non-disclosure agreement is typically required to obtain these from the vendor.

IBIS (I/O Buffer Interface Specification) has been proposed as a model for integrated circuits, which, approved as IEC 62014-1, has the following features:

- since electrical properties of I/O buffers are described in table format, disclosure of proprietary information such as process parameters is drastically reduced;
- it is easy to get IBIS models that are supported by many simulation tools;
- a public domain tool can convert SPICE models into IBIS models.

However, IBIS models seem to have the following problems:

- the modeling of power and ground currents is insufficient for accurate power and ground bounce analysis;
- since an IBIS model has only the final stage at output and input, it is difficult to model the effect of loading on circuit boards on output and input waveforms. The fixed model taken by IBIS has little flexibility for describing other circuitry;
- in order to simulate EMI with accuracy, more information such as material constant and three-dimensional structures is needed.

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1 Scope

The following items are considered to standardize the electrical modeling of input signals, output signals, power supply and ground terminals of integrated circuits, in order to provide for analysis of electrical characteristics of equipment.

1) To standardize in order to solve current problems and in order to extend capabilities of analysis, on the basis of results of the past standardization activities.
2) To define more flexible description rules for electric circuits in order to provide more accurate analysis of printed circuit board.
3) To introduce the concept of modeling levels to exchange relevant data for each application.
4) To enhance electrical modeling for packages and modules.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62014-1:2001, *Electronic design automation libraries – Part 1: Input/output buffer information specifications (IBIS version 3.2)*